Electronic Version
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Claims

[c1] What is claimed is:

An emission electron source comprising:

a first cathode electrode disposed on a substrate, the cathode electrode for providing a source of electrons;

an emitter layer being disposed over the said cathode electrode and formed from a composition of an embedding material and one or a plurality of vertically oriented and mono-dispersed nano-structures embedded therein, the emitter layer having a surface, parallel to which the nano-structures are truncated to substantially the same length and above the surface the nano-structures protrude for emitting electrons;

an insulator disposed over the emitter layer, the insulator having one or a plurality of apertures, each is aligned with and exposes one nano-structure in the emitter layer;

a second gate electrode disposed over the insulator and having one or plurality of apertures aligned with the apertures in the insulator, the gate electrode for controlling the emission of electrons through the apertures from the exposed nano-structures.

[c2] An electron source as recited in claim 1, wherein the gate aperture has a size substantially less than one micrometer.

[c3] An electron source as recited in claim 1, wherein the nano-structures have a surface density substantially higher than $10^6/cm^2$.

[c4] An electron source as recited in claim 3, wherein the nano-structures are grown from a plurality of catalyst dots patterned by depositing the said catalyst through a mask.

[c5] An electron source as recited in claim 4, wherein the mask includes membranes formed from ion-track etching and membranes formed from etching using an ion-track-etched membrane as a mask.

[c6] An electron source as recited in claim 1, wherein the nano-structures include nano-tubes, nano-wires, nano-fibers, and nano-cones.

[c7] An electron source as recited in claim 1, wherein the nano-structures are pre-fabricated and placed onto the cathode electrode by a self-assembly process.

[c8] An electron source as recited in claim 1, wherein the nano-structures are conductive and the embedding ma-

terial is nonconductive.

[c9] An electron source as recited in claim 8, wherein the conductive nano-structures are selected from a group of materials consisting of carbon, refractory metals and alloys, conductive ceramics, conductive ceramic composites, and doped semiconductors.

[c10] An electron source as recited in claim 9, wherein the carbon include carbon nano-tube, carbon nano-fiber, and carbon nano-cone.

[c11] An electron source as recited in claim 8, wherein the conductive nano-structures have a thin coating for enhanced field emission performance.

[c12] An electron source as recited in claim 8, wherein the conductive nano-structures comprise of a nonconductive core and a conductive shell.

[c13] An electron source as recited in claim 12, Wherein the nonconductive core is made from one of wide band gap semiconductors, including diamond, BN, AlN, AlGaN, GaN, GaAs, SiC, ZnO.

[c14] An electron source as recited in claim 1, wherein the nano-structures are non-conductive; and wherein the embedding material is conductive, the con-

ductive material for providing a means for electron transfer from the first electrode to the nano-structure for electron emission.

[c15] An electron source as recited in claim 14, wherein the non-conductive nano-structures are made from one of the wide band gap semiconductors, including diamond, BN, AlN, AlGaN, GaN, GaAs, SiC, ZnO.

[c16] An electron source as recited in claim 1, wherein the nano-structures are truncated by chemical mechanical planarization.

[c17] An electron source as recited in claim 1, wherein the insulator and the embedding material is the same dielectric material.

[c18] An electron source as recited in claim 1,
wherein the nano-structures are grown using a template and the said template is the embedding material.

[c19] An electron source as recited in claim 1,
wherein the first cathode electrode is configured as a plurality of electrically isolated electrodes;
wherein the nano-structure in the emitter layer is distributed in a pattern of a plurality of patches along the cathode electrodes;
wherein the second gate electrode is configured as a

plurality of electrically isolated electrodes, each intersecting with the plurality of cathode electrodes at the said patches of nano-structures, and having a plurality of apertures aligned with the apertures in the insulator at the intersections;
activation of a selected cathode and a selected gate electrode determines the patch of nano-structures that emit electrons.

[c20] A display comprising:
an electron source including: a first cathode electrode disposed over a substrate; an emitter layer being disposed over the said first electrode and formed from a composition of an embedding material and one or a plurality of vertically oriented and mono-dispersed nano-structures embedded therein, the emitter layer having a surface, parallel to which the nano-structures are truncated to substantially the same length and above the surface the nano-structures protrude for emitting electrons; an insulator disposed over the emitter layer and having one or a plurality of apertures, each is aligned with and exposes one nano-structure in the emitter layer; a second gate electrode disposed over the insulator and having one or plurality of apertures that are aligned with the apertures in the insulator; and
an anode plate including a transparent anode electrode

disposed over a glass substrate and a phosphor screen disposed over the anode electrode, and being positioned opposite to said electron source with a vacuum gap put therebetween; whereby electrons are emitted from said nano-structures by applying a voltage between said cathode and gate electrodes, and are made incident on said phosphor screen to make luminous said phosphor screen.

[c21] A display as recited in claim 20, wherein the gate aperture has a size substantially less than one micrometer.

[c22] A display as recited in claim 20, wherein the nano-structures have a surface density substantially higher than $10^6/cm^2$.

[c23] A display as recited in claim 20,
wherein the first cathode electrode is configured as a plurality of strip-like cathode electrodes extending substantially in the same direction in such a manner as to be spaced from each other at intervals in the transverse direction, each cathode strip for providing an independent source of electrons;
wherein the nano-structure in the emitter layer is distributed as a plurality of patches deposited over and along each cathode electrode;
wherein the second gate electrode is configured as a

plurality of strip-like gate electrodes extending in such a manner as to intersect said plurality of cathode electrodes at each said patches of nano-structures and to be spaced from each other at intervals in the transverse direction, and having a plurality of apertures aligned with the apertures in said insulator at the intersections, each gate electrode for controlling the emission of electrons through the apertures along the gate electrode; and wherein the anode electrode is configured as a plurality of strip-like anode electrodes each extending in such a manner as to be opposed to the corresponding one of the said second electrodes.

[c24] A method of fabricating an electron source, the method comprising:
providing a substrate;
depositing on the substrate a first conductive layer;
depositing one or a plurality of vertically oriented and mono-dispersed nano-structures over the first conductive layer;
comformally depositing a material to embed the nano-structures, forming an emitter layer with a surface above which ends of the nano-structures are to protrude;
truncating the nano-structures to substantially the same length by polishing the surface of the emitter layer;
etching back the embedding material from the polished

surface so that the ends of the nano-structures protrude above the surface for a small fraction of one micrometer;
conformally depositing an insulator over the surface of the emitter layer for a thickness substantially less than one micrometer, forming a post from each nano-structure;
depositing a second conductive layer over the insulator;
removing the insulator and the second conductive layer from the nano-structures to form apertures in the second conductive layer and in the insulator,
whereby nano-structures are exposed at the center of each of the aperture for electron emission and control.

[c25] A method as recited in claim 24,
wherein nano-structures are deposited over the first conductive layer by: depositing one or a plurality of nano-sized catalyst dots on the first conductive layer; and growing one nano-structure from each of the said catalyst dot.

[c26] A method as recited in claim 25, wherein nano-sized catalyst dots are deposited over the said first conductive layer through a mask.

[c27] A method as recited in claim 26,
wherein the mask includes membranes formed from ion-track etching and membranes formed from etching using

an ion-track-etched membrane as a mask.

[c28] A method as recited in claim 24,
wherein the nano-structures are grown by using a template; and
wherein the embedding material is the said template.

[c29] A method as recited in claim 24,
wherein the nano-structures are deposited over the first conductive layer using pre-fabricated nano-structures.

[c30] A method as recited in claim 24,
Wherein the nano-structures are truncated by chemical mechanical planarization.

[c31] A method as recited in claim 24,
wherein the second conductive layer is thinner than the insulator and deposited by a line-of-sight process such that it is only deposited on top of the posts and on the floor surface at the bottom of the posts; and
wherein the insulator and the second conductive layer are removed from the nano-structures by etching the insulator on the posts.

[c32] A method as recited in claim 24,
wherein the insulator and the second conductive layer are removed from the nano-structures by: removing the posts using chemical mechanical planarization to form

apertures in the gate electrode; and etching back the insulator using the gate electrode as a mask.

[c33] A method as recited in claim 24,
wherein the removal of the insulator and the second conductive layer from the nano-structures comprises of: spin coating the surface with a positive photo resist after the deposition of the second conductive layer; exposing the photo resist with a UV illumination in such a manner as to only the portions of the resist directly on top of the post is removed after resist development; etching the second conductive layer and the insulator through the resist mask; and stripping the photo resist.